JOHNS HOPKINS
WHITING SCHOOL
of ENGINEERING

INDEPENDENT STUDY/PROJECT APPROVAL FORM

(Engineering for Professionals)

Student Name: Khalil Blaine
Email Address: kblaine5@jh.edu
Phone: 682-261-0283

Course
Course Number/Title: EN.525.801 - Special Project I
Semester/Term: Summer 2026

Mentor/Instructor (Must be a current EP faculty member)
Name: John Penn
Email Address: jpenn3@jhu.edu
Phone:

Advisor
Name: Neil F. Palumbo
Email Address: npalumb1@jhu.edu
Phone:

Give a brief description of the independent study/project. Attach a second sheet as needed.
This form is available at: https://ep.jhu.edu/current-students/student-forms/

This special project covers the design, simulation, EM verification, and final die layout of a compact two-stage X-band MMIC power amplifier in Keysight ADS using the WIN MMIC course library. Work includes device screening, bias selection, small- and large-signal analysis, stability review, ADS Momentum verification of layout- sensitive structures, die floor planning, DRC review, and a final report/presentation. See attached signed DOE for the full scope, technical objectives, schedule, and deliverables.

Approvals (Obtain signatures in the order listed)

Student: Khalil A Blaine Date: 3/26/2026
Mentor/Advisor John Penn John E Penn Date: 3/26/2026
Advisor: Neil F. Palumbo Neil F. Palumbo Date: 3/26/2026
Program Chair: Cleon E. Davis Cleon Davis Date: 3/27/2026

Design of Execution

EN.525.801 - Special Project I

Design, Simulation, EM Verification, and Layout of a Two-Stage X-Band MMIC Power Amplifier in ADS

Student	Khalil Blaine
Program	M.S. in Electrical and Computer Engineering
Course	EN.525.801 - Special Project I
Term Requested	Summer 2026
Proposed Faculty Advisor	John Penn
Design Environment	Keysight ADS with the WIN MMIC course library
Primary Project Scope	Schematic design, circuit simulation, ADS Momentum EM verification, die floor planning, final layout, and documented DRC review
MMIC Die Envelope	Approximately 2.0 mm $\times$ 2.0 mm maximum
Future Evaluation Note	Any future 2 in $\times$ 2 in evaluation board would be a separate follow-on activity and is not a course deliverable

Request for approval. I am requesting approval to enroll in EN.525.801 as my final course during Summer 2026. The proposed work is a graduate-level MMIC design project completed entirely in ADS. The course endpoint is a coherent design package consisting of the amplifier schematics, simulation results, targeted ADS Momentum EM verification, die floor plan, completed layout, DRC review, and final written report. Fabrication, laboratory measurement, packaged hardware, and evaluation-board implementation are outside the required course scope.

1 Project Statement

This Design of Execution defines the technical scope, design objectives, verification flow, and deliverables for a special project in EN.525.801. The proposed work is the design, simulation, EM verification, and layout of a compact two-stage X-band MMIC power amplifier in ADS using the WIN MMIC course library. The amplifier will be centered at 10 GHz and will use a driver stage followed by a combined output stage sized for realistic X-band power performance within a constrained die area.

The project is intentionally die-centered. I will complete the design hierarchy, device screening, bias selection, linear and nonlinear simulation, layout development, targeted ADS Momentum EM verification, and DRC review in ADS. The work does not depend on laboratory access. It is structured so that the final report can document a disciplined path from initial circuit design to layout-aware review of the MMIC die.

2 Scope and Project End Point

In scope

- Device review and bias selection using the available WIN MMIC models.
- Schematic development of a two-stage MMIC power amplifier in ADS.
- Small-signal, large-signal, and stability verification.
- ADS Momentum EM verification of layout-sensitive passive and interconnect structures.
- Die floor planning, final layout, and documented DRC review.
- Final report and presentation material suitable for faculty review.

Out of scope

- Fabrication or tapeout.
- Wafer-probe measurements or packaged measurements.
- Laboratory board bring-up.
- Evaluation-board design, fabrication, or assembly as a required project deliverable.
- Measured results.

The intended course end point is a reviewed ADS design package rather than a fabricated hardware demonstration. Any future packaging effort or 2 in $\times$ 2 in evaluation board would be a separate activity after completion of the die-level design work.

3 Technical Objectives and Requirements

The table below defines a realistic baseline and a more ambitious target set for the simulated design. These values are intended to keep the project technically meaningful while remaining achievable within one summer term and within the constraints of the selected MMIC library.

Parameter	Baseline objective	Target objective	Verification
Useful operating band	Performance verified at 9.5 GHz, 10.0 GHz and 10.5 GHz	Useful behavior across approximately 9.5 GHz to 10.5 GHz	S-parameter and HB
Small-signal gain	At least 12 dB at 10 GHz	Approximately 15 dB at 10 GHz	S_{21}
Input return loss	Better than 8 dB at 10 GHz	Better than 10 dB across the main band	S_{11}
Output return loss	Better than 8 dB at 10 GHz	Better than 10 dB across the main band	S_{22}
Output power near compression	At least 26 dBm at 10 GHz	At least 27 dBm at 10 GHz	HB sweep
Saturated output power	At least 27 dBm	28 dBm to 30 dBm if supported by device size and bias	HB sweep
PAE at high drive	At least 20 % at 10 GHz	At least 25 % at 10 GHz	HB sweep
Bias range	All bias values kept within device-model limits	Design space to include drain bias near 8 V, if supported by the selected model	DC review
Stability	No simulated oscillatory behavior in the evaluated design space	Favorable K and μ trends over the design review sweep	Stability review
Die area	Compact die-level implementation	Approximately 2.0 mm × 2.0 mm maximum envelope	Die summary
Layout closure	Final ADS layout completed	Final layout reviewed with available DRC tools and documented status	Layout and DRC
EM verification	Critical structures selected for Momentum review	EM-backed retuning completed where needed	Momentum

Note on final values. All performance objectives in this DOE are simulation goals. The final transistor periphery, bias levels, and matching approach will be selected after device screening in ADS and may be adjusted to keep the design realistic within the available die area and the project schedule.

4 Proposed Amplifier Architecture

Figure 1 shows the planned signal path. The architecture is intentionally direct and suitable for a summer design effort: an input matching and stability section feeds the driver stage, the driver stage feeds the interstage match, and the interstage network excites a combined output stage that will be implemented with two matched output cells. Separate gate-bias and drain-bias networks will be maintained so that the final report can document the selected operating point and one secondary bias condition.

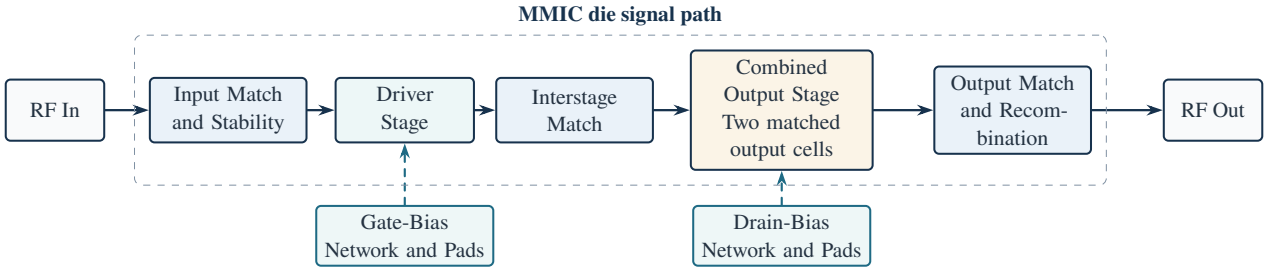

Figure 1: Proposed MMIC power-amplifier architecture.

5 Design Method and ADS Workflow

The design will be developed through a structured sequence of tasks so that each major decision can be reviewed, documented, and carried into layout with traceable justification.

5.1 Library Setup and Device Screening

I will begin by confirming the ADS workspace, validating the selected WIN library components, and building reusable benches for DC review, S-parameters, stability analysis, and harmonic-balance power sweeps. Candidate devices will then be screened according to gate width, current capability, gain, and their ability to support a compact die-level design at 10 GHz.

5.2 Output Stage Synthesis

The output stage will be designed first because it determines the power class of the final amplifier. I will use ADS large-signal simulation to identify practical source and load conditions at 10 GHz and then synthesize the output network around two matched output cells. The principal objective in this phase is to establish a realistic balance among output power, efficiency, die area, and stability.

5.3 Driver Stage and Interstage Design

Once the output section is defined, I will design the driver stage and the interstage network. The driver stage must provide sufficient gain and drive level without introducing unnecessary current consumption or an excessively narrow input match. The interstage match must transfer power cleanly into the output section while also supporting gain control and stability management.

5.4 Full Amplifier Optimization and Stability Review

After the individual sections are assembled into the full amplifier, I will optimize the input, interstage, and output networks together. This phase will include gain optimization, return-loss improvement, compression-behavior review, and the comparison of two bias conditions. Stability will be treated as a required design activity rather than a final check, with explicit review of low-frequency and out-of-band behavior.

5.5 ADS Layout, Momentum EM Verification, and DRC Review

The final schematic will be converted into a die-level layout in ADS. The layout phase will focus on pad planning, RF routing, ground strategy, via placement, symmetry in the output-stage region, and compact physical realization within the die-size objective. ADS Momentum will then be used to verify the passive and interconnect structures most likely to affect the final behavior, including RF pads, compact matching sections, routing discontinuities, and the output-stage combining region. Available DRC tools will be run and documented after the layout is stabilized.

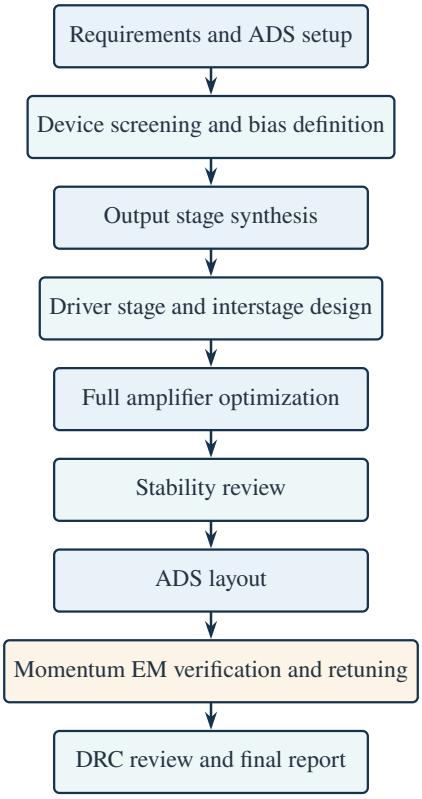

Figure 2: ADS execution workflow.

6 Die Floor Planning and Physical Constraints

The physical planning target for this project is an approximate maximum die envelope of 2.0 mm × 2.0 mm. The die must accommodate the RF probe-pad interfaces, dedicated bias pad groups, the driver section, the combined output stage, matching networks, ground-via structures, and practical RF routing. The floor-planning goal is therefore to keep the active signal path direct, to confine the output-stage region near the output side of the die, and to maintain orderly bias access without unnecessarily lengthening the RF route.

Physical planning item	Planned arrangement
RF probe-pad placement	RF input and RF output probe pads placed on opposing sides of the die to support clear signal flow and future die-level probing
Bias pad placement	Separate gate-bias and drain-bias pad groups positioned above the active signal path with short access routes into the driver and output-stage regions
Active-device placement	Driver stage located near the input side; combined output stage located near the output side to minimize the high-power output-path length
Matching-network placement	Input, interstage, and output matching sections placed sequentially between the RF pads and the active-device regions
Ground strategy	Perimeter via fence and local ground-via concentration in the output-stage region where required by the library rules
Future evaluation note	Any future package or 2 in × 2 in evaluation board would be a separate follow-on effort and is not a course deliverable

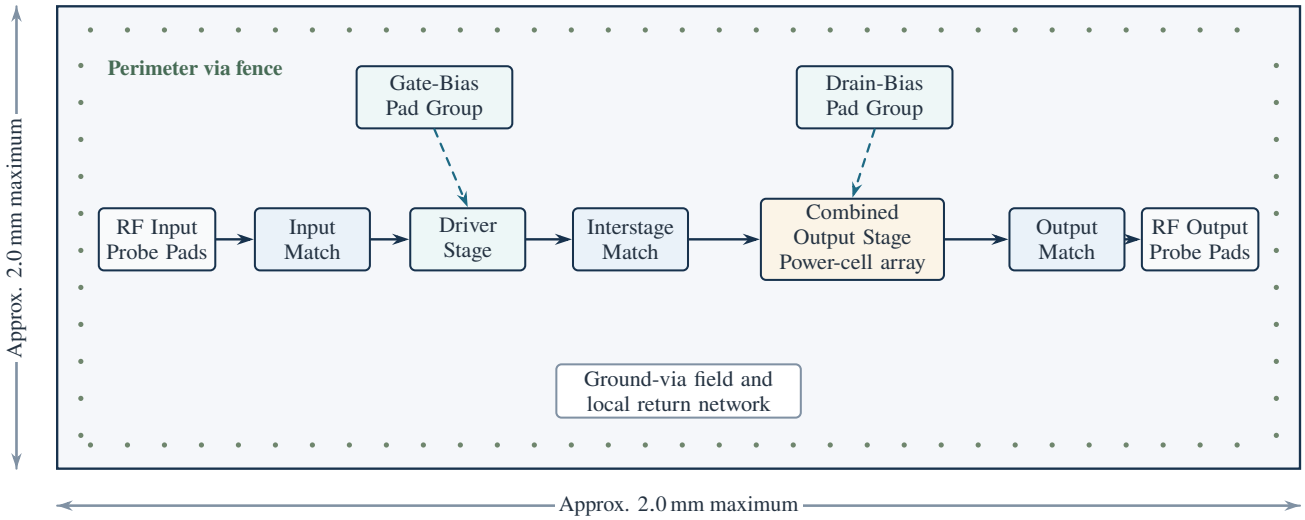

Figure 3: Conceptual die floor planning and pad organization for the proposed MMIC. The figure is schematic for readability and is not drawn to exact geometric scale.

7 Simulation, EM Verification, and Layout Review

The design will be verified in ADS through a structured simulation set. The goal is not only to generate plots, but also to show a disciplined path from circuit design to layout-aware review of the final amplifier.

Analysis set	Purpose	Planned output
DC bias review	Confirm operating points and current draw for the selected bias conditions	Bias tables and operating-point summaries
S-parameter simulation	Evaluate gain, input return loss, output return loss, and reverse isolation	Frequency plots across the design band
Stability analysis	Review K, μ, and low-frequency or out-of-band behavior	Stability plots and discussion of mitigation steps
Harmonic-balance power sweeps	Extract output power, P_{1dB}, gain compression, and PAE	Power-sweep plots at representative frequencies
EM comparison review	Compare pre-EM circuit behavior with EM-backed layout-aware response for critical structures	EM comparison figures and retuning summary
Bias comparison study	Compare the nominal bias condition and one alternate bias condition	Summary table of gain, power, current, and PAE
Layout review	Confirm die dimensions, pad placement, routing, and floor-plan consistency	Final layout figures and die summary
DRC review	Document the available layout-rule review completed in ADS	DRC result summary in the final report

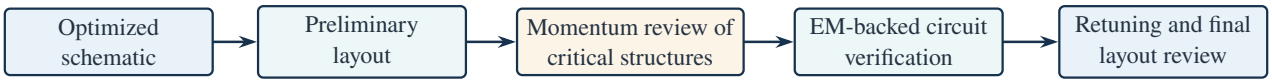

Figure 4: Planned ADS Momentum verification sequence.

8 Deliverables and Advising Plan

D1. Approved Design of Execution.

D2. ADS project archive with hierarchical schematics and reusable test benches.

D3. Device-screening summary and documented bias selections.

D4. Small-signal, large-signal, stability, and EM-comparison figures.

D5. Final MMIC die layout with floor-planning summary and documented DRC status.

D6. Final written report suitable for faculty review.

D7. Final presentation package.

Weekly one-hour Zoom meetings with the faculty advisor are planned throughout the summer term. Each meeting will be used to review the current milestone, identify design blockers, and confirm the next week's work.

9 Proposed Summer Schedule

The schedule below assumes an approximately ten-week summer execution window.

Week	Planned work	Main output
1	Finalize specifications, establish ADS workspace, confirm device options, and set up reusable simulation benches.	Requirements memo
2	Screen driver and output devices; review safe bias range and current draw.	Device shortlist
3	Complete output-stage study and choose preliminary operating point.	Output-stage summary
4	Build driver stage and input match; begin interstage development.	Driver-stage schematic
5	Integrate the full amplifier and complete initial S-parameter and HB verification.	First full result set
6	Refine gain, matching, and compression behavior; compare nominal and alternate bias conditions.	Updated schematic and bias comparison
7	Complete stability review and prepare the design for layout.	Stability review package
8	Build final ADS layout and confirm die floor plan.	Layout draft
9	Run targeted ADS Momentum EM verification and document any required retuning.	EM-backed design review
10	Complete DRC review, final report, and presentation package.	Final submission package

10 Risks and Mitigation

Wideband stability can limit achievable gain and power. Stability will be reviewed early in the design process rather than after the amplifier has been fully optimized. Bias-feed parasitics, damping measures, and matching adjustments will be introduced only when justified by simulation evidence.

Die area can become the dominant physical constraint. Device periphery, passive size, and routing length will be traded together rather than independently. The floor plan will be maintained alongside the schematic development so that the design remains realistic for a compact MMIC die.

EM results may shift the tuned circuit response. The Momentum review is included before the final report stage so that layout-sensitive structures can be retuned and the EM-backed results can be documented in the final submission.

11 Requested Approval

I respectfully request approval to enroll in EN.525.801 - Special Project I during Summer 2026 and to complete the project described in this Design of Execution under faculty supervision. I am prepared to provide weekly status updates, to review milestones with the faculty advisor throughout the term, and to submit the full ADS design package and final report by the end of the summer session.

Student

Khalil Blaine 3/20/2026

Signature and Date

Faculty Advisor Agreement

John Penn

I agree to advise this project. Signature and Date